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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	**John LeRoy Parker, Jr., et al.**	)
		)
Serial No.:	**Not Yet Assigned**	)
		)
Examiner:	**K. Rinehart**	)
		)
Filed:	**Herewith**	)
		)
For:	**VIA CONNECTOR AND METHOD OF MAKING SAME**	)

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Commissioner for Patents
P.O. Box 1450
Arlington, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

List of Sections Forming Part of This Information Disclosure Statement

The following sections are being submitted for this Information Disclosure Statement:

1. [X] Preliminary Statements

2. [X] Form PTO-1449 (modified)

3. [X] Statement as to Information Not Found in Patents or Publications

4. [X] Identification of Prior Application in Which Listed Information Was Already Cited and for Which No Copies Are Submitted or Need Be Submitted

5. [ ] Cumulative Patents or Publications

6. [ ] Copies of Listed Information Items Accompanying this Statement

7. [ ] Concise Explanation of Non-English Language Listed Information Items

   7A. [ ] EPO Search Report

   7B. [ ] English Language Version

8. [ ] Translation(s) of Non-English Language Documents

9. [ ] Concise Explanation of English Language Listed Information Items (Optional)

10. [X] Identification of Person(s) Making this Information Disclosure Statement

Section 1. Preliminary Statements

Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made (37 C.F.R. § 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability or that no other material information exists.

The filing of this information disclosure statement shall not be construed as an admission against interest in any manner. Notice of January 9, 1992, 1135 O.G. 13-25, at 25.

Section 2. Form PTO-1449 (Modified)

[X] A Completed Form PTO-1449 (Modified) is attached hereto.

Section 3. Statement as to Information Not Found in Patents or Publications (Information Not Listed in Form PTO-1449(Modified)

Increasing levels of integration of integrated circuit (IC) chips reduces the chip count of functional circuit, while significantly increasing the input/output (IO) count of the individual integrated circuits making up the functional circuit. This drive for increasing circuit and component density in the individual IC chips leads to a parallel drive for increased circuit and component density in the printed circuit boards carrying the chips and in the assemblies using them.

Typically, a conventional printed wiring board carries Ics as well as other discrete electronic components and circuit elements, which are interconnected to provide the particular electronic circuit functions. In the prior art, those Ics, discrete electronic components, and circuit elements are usually bonded to the printed wiring board using vias or through holes formed in the printed wiring board through which lead wires may be inserted and soldered to the board. However, there have been advances in surface mounting technology widely employed in the printed wiring board manufacturing field. This technology permits an IC to be mounted together with it s associated elements on the printed wiring board without forming any through holes or vias in the board. Thus, Ics and other on-chip elements may be mounted on a surface mount land or chip land directly without using the through holes or vias.

To provide for the interconnections between the on-chip elements on the surface mount land on one side and a circuit on the opposite side of, or within, the printed wiring board, the appropriate vias are often provided remotely from the surface mount land, and any wiring pattern required for interconnecting the elements by way of the vias must be formed on the surface of the base plate.

Thus, according to the prior art, the surface mount land or chip land and the vias or through holes are provided at different locations on the printed wiring board. As the size of each of the Ics and other elements is reduced, a corresponding reduction in the size of the surface mount land is required so that required board space is minimized. The wiring pattern that includes leads drawn out from the surface mount land and distributed across different locations must be accordingly fine, but technically, this is practically difficult to acheive. It is also difficult to secure the space required for wiring the leads. In particular, for double-sided high-density wiring pattern implementation, this space limitation poses a problem.

The vias formed in the printed wiring board are exposed on each of the opposite sides of the board. When leads are inserted through the corresponding vias, and the associated circuit components are fixed by the board in solder, surplus solder may flow through the vias, thereby reaching the components on the surface mount land.

In other conventional circuit boards which carry wiring patterns formed on two opposing major surfaces, vias or through holes are formed at desired positions after conductive layers are formed on the entire surface of the opposing major surfaces of the circuit board. Inner surfaces of the thus formed vias are coated with plated layers through the use of a chemical plating method or a chemical/electrical plating method, thereby providing electrical communication between the conductive layers formed on the two major surfaces or internal to the circuit board by way of the plated layers.

The vias are formed through the use of a drilling method or a punching method. Therefore, there is the possibility that the circuit board or the conductive layers become distorted during the formation of the through holes. The thus formed distortion will adversely influence the formation of the plated layers so that an effective electrical connection cannot be achieved between the two conductive layers. In addition, fine wiring patterns cannot be formed near the vias due to the distortion of the conductive layers. Thereafter, the conductive layers are shaped in a desired configuration to obtain wiring patterns formed on both of the major surfaces of the circuit board.

Another example of prior art via connectors is disclosed in U.S. Patent No. 3,601,523 "THROUGH HOLE CONNECTORS" to Arndt, issued on August 24, 1971, wherein a conductive adhesive is disposed in the through holes or vias for providing electrical communication between the conductive layers formed on both of the major surfaces of the circuit board. In the device of the '523 patent, the vias are formed after the conductive layers are formed on both of the major surfaces of the circuit board and, therefore, there is a possibility that the conductive layers will become distorted near the vias. Moreover, in the '523 patent, electrical communication between the conductive layers and the conductive adhesive is achieved only through the use of the thickness of the conductive layer. In addition, the conductive adhesive is exposed to the ambience. Therefore, the shaping of the wiring pattems must be conducted through the use of a dry film or a resist sheet.

The increased circuit and component density in the printed circuit boards makes the ability to locate either solder surface mount components or place additional circuitry layers directly above conductive vias highly desirable. This

is especially the case when the density of the vias required to service the I/O's of the surface mount components is such that there is no surface area available for attachment pads interstitial to the through hole grid.

The problem is especially severe with fine pitch ball grid array components and flip chip attach integrated circuits. Soldering of these surface mount components to the surface pads, i.e., lands, of conventional vias is highly undesirable. This is because the solder used for assembly tends to wick down into the vias. The result is low volume, unreliable solder joints.

One solution that has been proposed is filling the vias. However, known methods of filling vias of printed circuit boards have deficiencies. For example, they suffer from bleed of the resin component of the fill material along the surface of the boards. This resin also bleeds into the holes which are not to be filled. This leads to short circuits and to soldering defects during assembly.

Thus, conductive vias provide aa immediate connection from a surface mounted device to the core of a printed circuit board, thereby avoiding inefficient fan out routing patterns that consume space on the outer layers of the multilayer board. These designs, however, present significant assembly problems. Small vias act as entrapment sites for materials that can eventually re-deposit onto the host surface mount land and cause both assembly and reliability problems. Also, these vias act as unintended reservoirs for solder paste that is stenciled onto the surface mount land and used to attached an electronic device to the board. Consequently, an allowance must be made of the solder paste that will be captured by the via and will not be available for the solder joint formed between the device and the board. Typically, the same allowance is rnade for each via by slightly enlarging the solder paste stencil aperture for each surface mount pad containing a via by some common amount. Because the precise allowance needed varies to via to via, this method leads to an insufficient amount of paste for some lands causing poor solder joints and an over-abundance of solder on others causing solder shorts; both of which unfavorably impact assembly yields.

Another example of prior art via connectors is disclosed in U.S. Pat. No. 5,557,844 'METHOD OF PREPARING A PRINTED CIRCUIT BOARD" to Bhatt et al., issued on Sep. 24, 1996 and assigned to IBM, (referred to herein as "IBM"), wherein a printed circuit board has two types of plated through holes, filled and unfilled. The two types of through holes are fomed at different times during the manufacturing process. The through holes that are to be filled are formed first, and the through holes that remain unfilled are later formed using the location of the first through holes for registration.

Because all the holes are not formed simultaneously, misregistration of subsequently applied wiring patterns with the holes is likely as a result of tolerance build-ups. Moreover, IBM uses an electroless deposition for the plating of the sidewalls of the through holes, thus limiting the layer thickness to approximately 0.2 mils.

Although the art of vias and through hole connectors on printed circuit boards is well developed, there remain some problems inherent in this technology, particularly the vias and through hole connectors acting as solder reservoirs, thus leading to soldering defects, and the electrical conductivity of the vias. Therefore, a need exists for a via or through hole connector that overcomes the drawbacks of the prior art.

Section 4. Identification of Prior Application in Which Listed Information Was Already Cited and for Which No Copies Are Submitted or Need Be Submitted

This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application Serial No. **09/045,615**, filed on **March 20, 1998**, now abandoned.

(complete the following, if applicable)

[ ] This application also relies, under 35 U.S.C. 120, on the earlier filing date of prior application Serial No. _____, filed on _____ (date).

The following references were submitted to, and/or cited by, the Office in the prior application(s) and therefore, are not required to be provided in this application:

Section 5. Cumulative Patents or Publications

STATEMENT

_____ is cumulative of the following patents or publications listed on Form PTO-1449:

In accordance with 37 C.F.R. § 1.98(c), a copy of only ____ is being submitted with this Information Disclosure Statement.

Section 6. Copies of Listed Information Items Accompanying this Statement

Legible copies of all items listed in Form PTO-1449 (Modified) accompany this information disclosure statement.

[ ] Exception(s) to above:

[ ] Items in prior application from which an earlier filing date is claimed for this application, as identified in Section 4.

[ ] Cumulative patents or publications identified in Section 5.

Section 7. Concise Explanation of Non-English Language Listed Information Items

Section 7A. Concise Explanation of Non-English Language Listed Information Items - EPO Search Report

The relevance with respect to the following citations listed on Form PTO-1449:

is submitted on the basis of accompanying:

(check the appropriate item)

[ ] EPO search report that is in the English language,

[ ] EPO search report that is not in the English language and that is accompanied also by an English language version of the EPO search report,

that issued on the corresponding European patent application.

Section 7B. Concise Explanation of Non-English Language Listed Information Items - English Language Version of EPO Search Report

Section 8. Translation(s) of Non-English Language Documents

[ ] Submitted herewith is an English translation of the following foreign language patents, publications or information or of those portions of those patents, publications or information considered to be material:

(complete the following, if applicable)

[ ] No English language translations of the foreign language parents, publications or information or parts thereof are readily available, except for those listed above.

[ ] The following foreign language documents submitted are believed to be the equivalent or substantial equivalent of the English language documents identified below, which are also submitted herewith.

Section 9. Concise Explanation of English Language Listed Information Items (OPTIONAL)

Section 10. Identification of Person(s) Making this INFORMATION DISCLOSURE STATEMENT

The person making this statement is the attorney who signs below on the basis of the information:

[ ] supplied by the inventor(s)

[ ] supplied by an individual associated with the filing and prosecution of this application (37 C.F.R. § 1.56(c)).

[X] in the attorney's file

Respectfully submitted,

Marc Brockhaus

Marc A. Brockhaus, Reg. No. 40,923
DUNLAP, CODDING & ROGERS, P.C.
P.O. Box 16370
Oklahoma City, Oklahoma 73113
(405) 607-8600 - telephone
(405) 607-8686 - telefax

Attorney for Applicant

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	10/632,576
Filing Date	07/28/03
First Named Inventor	John LeRoy Parker, Jr. et al.
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	8245.057

U. S. PATENT DOCUMENTS

EXAM INIT.	Cite No. 1	U.S. PATENT NUMBER Number	Kind Code² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	3,099,608		Radovsky et al.	07-30-1963	
	AB	3,471,631		Quintana	10-01-1969	
	AC	3,601,523		Arndt	08-24-1971	
	AD	4,131,516		Bakos et al.	12-26-1978	
	AE	4,323,593		Tsunashima et al.	04-06-1982	
	AF	4,325,780		Schulz, Sr. et al.	04-20-1982	
	AG	4,383,363		Hayakawa et al.	05-17-1983	
	AH	4,435,611		Ohsawa et al.	03-06-1984	
	AI	4,908,940		Amano et al.	03-20-1990	
	AJ	4.911,796		Reed	03-27-1990	
	AK	5,239,746		Goldman	08-31-1993	
	AL	5,243,142		Ishikawa et al.	09-07-1993	
	AM	5,277,787		Otani et al.	01-11-1994	
	AN	5,293,504		Knickerbocker et al.	03-08-1994	
	AO	5,319,159		Watanable et al.	06-07-1994	
	AP	5,340,947		Credie et al.	08-23-1994	
	AQ	5,421,083		Suppelsa et al.	06-06-1995	
	AR	5,435,480		Hart et al.	07-25-1995	
	AS	5,463,191		Bell et al.	10-31-1995	
	AT	5,473,120		Ito et al.	12-05-1995	
	AU	5,481,795		Hatakeyama et al.	01-09-1996	
	AV	5,510,580		Shiral et al.	04-23-1996	

Examiner Signature:	Date Considered:

EXAMINER: Initial if citation considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant. **Place of Publication refers to name of publication in which the information was published.

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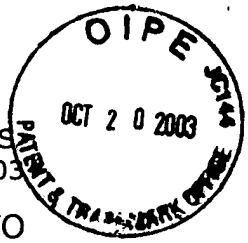

Substitute for form 1449A/PTO

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(use as many sheets as necessary)

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Application Number	10/632,576
Filing Date	07/28/03
First Named Inventor	John LeRoy Parker, Jr. et al.
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	8245.057

U. S. PATENT DOCUMENTS

EXAM INIT.	Cite No. 1	U.S. PATENT NUMBER Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	BA	5,527,998		Anderson, et al.	06-18-1996	
	BB	5,557,844		Bhatt et al.	09-24-1996	
	BC	5,571,593		Aridt et al.	11-05-1996	
	BD	5,585,673		Joshi et al.	12-17-1996	
	BE	5,662,987		Mizumoto et al.	09-02-1997	
	BF	5,674,787		Zhao et al.	10-07-1997	
	BG	5,761,803		St. John et al.	06-09-1998	
	BH	5,879,787		Petefish	03-09-1999	
	BI	5,958,562		Tsuji et al.	09-28-1999	
	BJ	5,960,538		Kawakita, et al.	10-05-1999	
	BK	5,977,490		Kawakita, et al.	11-02-1999	
	BL	6,079,100		Farquhar et al.	06-27-2000	
	BM	6,195,883		Bhatt et al.	03-06-2001	
	BN	US-2001/0027605		Nabetomoto et al.	10-11-2001	
	BO	US-6323439		Kambe et al.	11-27-2001	
	BP	US-2002/0016018		Oka et al.	02-07-2002	
	BQ	US-2002/0020557		Nishi et al.	02-21-2002	
	BR	US-2002/0035784		Koyama et al.	03-28-2002	
	BS	6,418,616		Bhatt et al.	07-16-2002	

Examiner Signature:	Date Considered:

EXAMINER: Initial if citation considered, whether or not citation is in conformance and not considered. Include copy of this form with next communication to applicant. **Place of Publication refers to name of publication in which the information was published.

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FOREIGN PATENT DOCUMENTS

EXAM INIT.	Cite No. 1	Foreign Patent Document: Office 3	Foreign Patent Document: Number 4	Foreign Patent Document: Kind Code5 (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

U.S. and Foreign: [1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard St.3). [4] Form Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard St. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

EXAM INIT.		NON PATENT DOCUMENTS
		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published

Non Patent Documents: [1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature:	Date Considered: